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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,666	07/29/2003	Wuu Yean Tay	4249.9US (99-0543.09US)	6475

24247 7590 03/08/2004

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,666	TAY ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0703*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of U.S. Patent No. 6,600,335. Although the conflicting claims are not identical, they are not patentably distinct from each other because although claims 1-7 of the claimed application have been amended with some changes it would have been obvious to still read on the claims 1-7 of US Patent No. 6,600,335 since the scope of both claims are still similar.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the

various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art of figs. 1 and 4 in view of Mennitt et al (5334857).

Regarding claim 1, the admitted prior art of figs. 1 and 4 discloses a ball grid array chip package (10) comprising a substrate (12) having a first surface (22) and a second surface (32) [see prior art fig. 2] opposite the first surface (22) and having an aperture (14) in communication with the first (22) and second (32) surfaces of the substrate (12); attaching a semiconductor device (represented as die 16) having an active surface (18) with a plurality of bond pads (20) thereon to one of the first (22) and second (32) surfaces of the substrate (12) with the plurality of bond pads (20) exposed within the aperture (14) of the substrate (12); providing a plurality of ball grid array connective elements (28) on one of the first (22) and the second (32) of the substrate (12); providing a plurality of substrate bond pads (24) on one of the first (22) and second (32) of the substrate (12); providing a plurality of bond wires (30) connecting the bond pads (20) on the active surface (18) of the semiconductor device (16) with the bond pads (24) of the substrate (12); providing a first plurality of circuit traces (26) connecting the substrate bond pads (24) with the connective elements (28); placing [see prior art fig. 4] the at least one ball grid array semiconductor package (10) in a burn-in and test apparatus

(represented as testing tool 40) having a plurality of test probes (48); burn-in and testing the semiconductor device (16) by applying and routing electrical energy by way of the plurality of test probes 48) [see page 2 –page 3 line 21 and page 3 line 30- page 5 line 6]. However, the prior art does not disclose test pads as claimed. Mennitt et al teaches a ball grid array semiconductor package (see fig. 2) having at least one test pad (not number but located between the inside of cut line B and outside cut line A) on a severable portion of the substrate (12) (see column 5 lines 13-46). Further, Mennitt teaches that the addition of the test pads is advantageous because after testing, the test pads may be eliminated to reduce the size of the device (see column 5 line 40-43). It would have been obvious to one ordinary skill in the art at the time the invention was made to provide the package of the admitted prior art with test pads on a severable portion of a substrate as taught by Mennitt et al for the purpose of testing the device and then eliminating the test pads to reduce the size of the device.

Regarding claim 2, Mennitt discloses [see fig. 2] the plurality of test pads (not number but located between the inside of cut line B and outside cut line A) comprising arranging the test pads in a thin small outline package pin-out pattern.

Regarding claim 3, the admitted prior art of fig. 1 discloses providing at least one of the first and second pluralities of circuit traces (26) comprising performing at least one of the first and second pluralities of circuit traces (26) inherently on a tape (not shown) and adhering [via adhesive 34] at least portion of the tape onto at least portion of the substrate (12).

Regarding claim 4, Mennitt discloses [see fig. 2] severing at least one of the plurality of test pads from the substrate (12) after burning-in and testing [see column 5 lines 29-36].

Regarding claim 5, the admitted prior art of fig. 4 discloses conducting the burn-in and testing of the semiconductor device (16) in test tooling (40) comprising a ball grid array semiconductor package holder (42) and a probe head (46) containing the plurality of test probes (48) arranged in a pattern complementary to the connective elements (28).

Regarding claim 6, the admitted prior art of fig. 1 discloses attaching the semiconductor device (16) and the plurality of connective elements (28) to the same surface of the first surface (22) and the second surface (32) of the substrate (12).

Regarding claim 7, the admitted prior art of fig. 1 discloses attaching the plurality of substrate bond pads (24) on one of the first surface (22) and the second surface (32) of the substrate (12) opposite to which the semiconductor device (16) and the plurality of connective elements (28) are attached.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (517) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
March 1, 2004

David A. Zarneke
Primary Exam
AU 2824
3/3/4